RAYS TECHNOLOGY

8T8R RF Direct-Sampling SDR Digital Core Board

Wideband Multi-Channel Platform for Wireless Communications, Spectrum Monitoring, Radar, Remote Sensing and Research

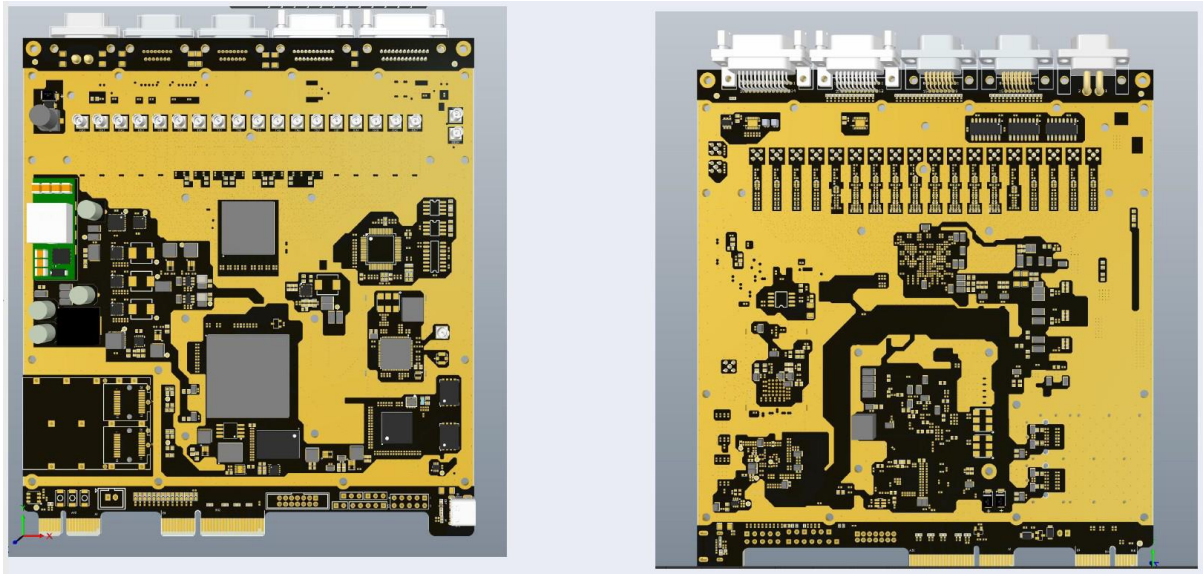
8 TX | 8 RX | 14-bit RF ADC/DAC | FPGA Processing

Product Brochure v7 | October 2026

Product Overview

The RAYS TECHNOLOGY 8T8R RF Direct-Sampling SDR Digital Core Board is a multi-channel software-defined radio platform based on the 8T8R + 2FB RF transceiver architecture and Kintex UltraScale+ XCKU5P FPGA processing. It integrates eight 14-bit ADC channels and eight 14-bit DAC channels for parallel RF signal acquisition, generation and real-time digital processing. The platform is positioned for SDR, 6G sensing and communication research, radar and other wideband RF research applications.

SDR Core Board Appearance



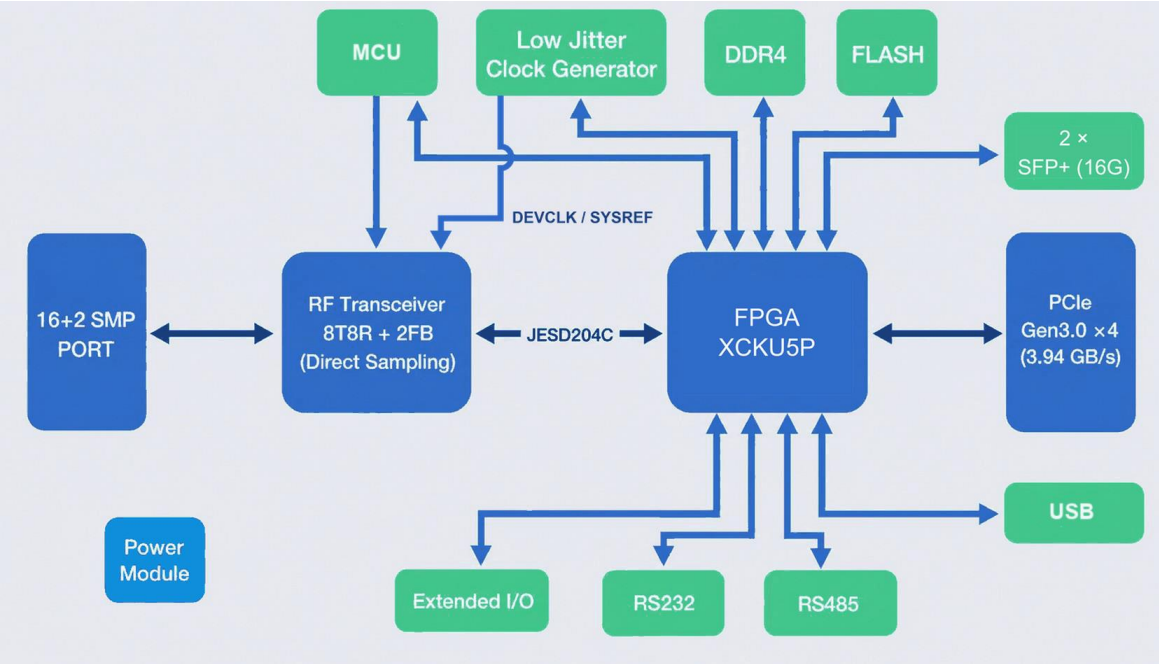
CAD renders, front and rear

Key Features

- 8T8R + 2FB direct-sampling transceiver: 8 transmit, 8 receive and 2 feedback channels.
- 8 × 14-bit ADC channels with a maximum sampling rate of 5.8 GSPS.
- 8 × 14-bit DAC channels with a maximum sampling rate of 9.85 GSPS.
- RF direct-sampling architecture for wideband signal acquisition and generation.
- Receive 20 MHz to 10 GHz (design target); transmit range to be characterised.
- Digital tuning: down-conversion and NCO in the RF-sampling transceiver, further processing in the FPGA; per-channel bandwidth set by decimation and the JESD204C lane budget.
- Kintex UltraScale+ XCKU5P FPGA for real-time parallel signal processing.
- JESD204C high-speed converter-to-FPGA data interface.
- PCIe Gen3 ×4 host interface and dual 16G SFP+ optical interfaces for data exchange.
- Clock architecture designed for multi-channel synchronized sampling.
- Power consumption: typical ≤ 40 W (design target).

System Architecture

The platform integrates an 8T8R RF direct-sampling transceiver subsystem with a Kintex UltraScale+ XCKU5P FPGA. The RF section and FPGA communicate through JESD204C. The digital processing subsystem is supported by DDR4, Flash memory and a low-jitter clock generator, with PCIe, SFP+, USB, RS232, RS485 and extended I/O connectivity for host integration and system expansion.



8T8R + 2FB RF direct-sampling architecture with JESD204C and XCKU5P FPGA processing

Technical Specifications

Parameter	Specification
Channel Configuration	8T8R + 2FB: 8 TX, 8 RX, 2 feedback
RF Architecture	RF direct-sampling transceiver
ADC	8 channels, 14-bit
Maximum ADC Sampling Rate	5.8 GSPS (converter maximum)
DAC	8 channels, 14-bit
Maximum DAC Sampling Rate	9.85 GSPS (converter maximum)
Frequency Range	Receive 20 MHz to 10 GHz (design target); transmit range to be characterised
Per-Channel Bandwidth to FPGA	Set by decimation and JESD204C lane budget; to be published when characterised
FPGA	Kintex UltraScale+ XCKU5P
FPGA Resources	475K logic cells; 1,824 DSP slices
Converter Interface	JESD204C
Host Interface	PCIe Gen3 ×4 (4 × 8 GT/s, ≈31.5 Gb/s after 128b/130b encoding)
Optical Interface	2 × 16G SFP+
Additional Interfaces	USB, RS232, RS485, Extended I/O
Operating Temperature	-40 °C to +70 °C (design target)
Power Consumption	Typical ≤ 40 W (design target)
Module Size	165 mm × 150 mm × 30 mm
Weight	700 g

Application Scenarios

- 6G sensing and communication research.
- Multi-channel synchronized RF acquisition and processing.
- Wideband signal acquisition and real-time FPGA signal processing.
- Radar signal acquisition and waveform generation.
- RF sensing and multi-channel signal research.
- SDR algorithm development and research platforms.

Why Choose the 8T8R SDR Core Board?

- Eight-channel ADC/DAC architecture for parallel multi-channel RF processing.
- Direct-sampling architecture digitizes and generates RF signals directly: no analogue mixer or local oscillator, so no LO leakage or analogue I/Q imbalance. Remaining spurs (converter interleaving, NCO spurs, clock jitter) are to be characterised.
- High-speed 14-bit ADC/DAC resources support broadband acquisition and waveform generation.
- Kintex UltraScale+ XCKU5P FPGA supports parallel real-time signal processing.
- PCIe Gen3 ×4 and dual 16G SFP+ interfaces support high-speed data exchange.

Development Status

As of October 2026 the board hardware is built. The FPGA firmware and the PCIe streaming data path are in development. Host software with a board simulator and a Windows PCIe driver based on the XDMA reference driver exist. No measured RF performance is published yet: figures in this brochure are converter capabilities or design targets and will be updated as the board is characterised. Remaining spurs and channel-to-channel alignment are to be characterised.

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Product information subject to configuration and customization.

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